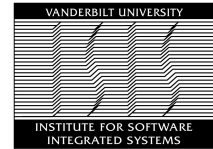


SPML: Signal Processing Modeling Language and Toolchain for Developing High-Performance Embedded Signal Processing Applications¹

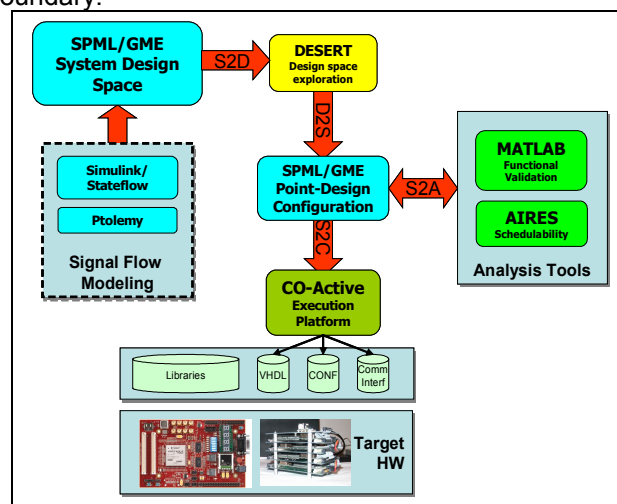


Summary of Features

SPML is a domain-specific modeling language to model and construct applications running on a heterogeneous, embedded platform, composed of high-performance FPGA-s with embedded processor cores, ASIC-s, Digital Signal Processors, and RISC processors. The language is supported by a set of integrated tools that fully support a model-based design process: component modeling, system architecting and modeling, hardware-software co-design, design-space exploration, code synthesis and execution.

The SPML Toolchain implements a model-based design process. The toolchain includes the following elements (as illustrated in the figure below):

- Component and System Modeling Tool (SPML/GME visual model editor) that supports creation of component models, system architecture models which describe a hierarchical organization of components and component interactions, heterogeneous hardware models that describe the embedded platform – FPGA-s, DSP-s, ASIC-s, and GPP-s, component allocations, etc. A key feature of the tool is the ability to model design alternatives. Thus the system design model can capture a design space for the application in the form of hierarchically arranged alternatives.
- Design Space Exploration Tool (DESERT) allows exploration and pruning of the large design spaces that are captured in the SRML models, based on user-supplied performance and resource constraints.. This gives the ability to obtain a custom solution from a generic and large design space based on the specific requirements in a largely automated manner. In this type of hardware-software co-design application DESERT also provides an automated way of partitioning functionality across hardware-software boundary.
- Design Simulation Tool (Matlab currently) that supports a functional simulation of the signal processing application.
- Design Analysis Tools (AIRES² currently) that supports event and timing analysis (including schedulability).
- CoActive Build and Execution platform that supports the synthesis of hardware (VHDL glue code) and software (communication maps, schedule tables), and interface for communication across hardware/software boundary.



SPML Tool-chain

The tools are integrated using an Open Tool Integration Framework that allows including other tools into the toolchain if needed.

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² Developed by University of Michigan.