Abstract
Development Environment for Dynamically Reconfigurable Embedded Systems

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Modern high-performance embedded systems face many challenges: Systems must function in rapidly changing environments; Power/size constraints limit hardware size; and extreme performance requirements demand algorithm-specific architectures. Missile Automatic Target Recognition is an example, where 10's of GFLOPS must fit into a ½ cu. ft. volume. Reconfigurable computing devices offer the chance to address these challenges with architectures that change in response to the changing environment. Hardware architectures are required that can structurally adapt, tuning themselves for each model of operation to achieve high performance with changing algorithms. The primary difficulty in this approach lies in system design. This paper describes high-level design tools that are being developed to assist the engineer in capturing designs and automatically generating functional systems.

A *model-integrated* approach is used in the design capture and synthesis of these systems. The Model-Integrated approach defines a domain-specific graphical system design environment, customized to the needs of the reconfigurable systems designer. The tools capture system requirements, algorithm design information and alternatives, and the resources available for system implementation. This information is represented as a set of *Multi-Aspect Models*. A model interpretation process uses these models to create a fully functional system. This process generates hardware/software architecture specifications, executable/synthesizable code, and a run-time Configuration Manger allowing dynamic adaptation to changing environments while the synthesized system is on-line. The synthesis process optimizes hardware/software architectures for user-definable cost functions such as weight, power, algorithmic accuracy and flexibility.

The target systems are built on a heterogeneous computing platform including configurable hardware, ASIC and general-purpose processors, and DSP's. An underlying execution environment supports system execution with a common virtual environment. The runtime supports the execution of a Dataflow specified computation, where the computational elements are distributed over the heterogeneous architecture. The runtime environment enables seamless integration of the different implementation technologies. The runtime environment also manages the dynamic system reconfiguration, including software reconfiguration for the parallel DSP's and hardware reconfiguration for the FPGA's in the system. The Runtime environment is described in a companion paper.

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